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Thermal Dip Pen Nanolithography

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Introduction: The steady shrinking of integrated circuits demands constant innovation. Though ever-greater resolution remains the foremost goal, many new abilities are also needed—the reduction of toxic by-products ("green chemistry"), integration of heterogeneous materials (e.g., organic and inorganic) into a single structure, and the production of just a few integrated circuits at low cost. We are developing a new lithographic approach, thermal Dip Pen Nanolithography (tDPN), to both achieve greater resolution and address many of these secondary needs.[1,2]

Although tDPN can create nanoscale structures, in principle it works as simply as a soldering iron. The heart of the device is a custom-fabricated *heatable* atomic force microscope (AFM) tip, coated with a material (i.e., the "solder" or "ink") that is solid at room temperature. When melted, the ink flows from the tip onto the surface (Fig. 1). The use of meltable inks has many benefits. Since the ink's fluidity is controlled by the tip temperature, writing may be turned on or off and the deposition rate easily varied. Secondly, one can write new layers on top of previously deposited—now solid—layers to create complicated three-dimensional structures. Finally, tDPN can be performed in vacuum, making it compatible with conventional semiconductor device fabrication.

Current Capabilities of tDPN: We have used tDPN to deposit metals, polymers, and self-assembling monolayers. The technique is particularly powerful for polymer deposition. Because tDPN requires only that the polymer melt before it decomposes, a wide range of polymers may be used. To date, an insulating polymer, Mylar, and two conducting polymers, MEH-PPV and PDDT, have all been successfully deposited.

An important aspect of tDPN is that ink can be deposited with sufficient thermal energy to organize into well-formed monolayers before solidifying. This capability is illustrated in Fig. 2, which shows the deposition of poly(3-dodecylthiophene) (PDDT), a conducting polymer used in organic-based electronics. The coated tip was heated and scanned over a rectangular area to deposit a polymer film, precisely a *single* molecular layer thick onto the SiO_2 substrate. A second pass added a second monolayer without disturbing the first. The stepwise nature of the deposition is clearly seen in the averaged cross-section (Fig. 2(b)). The thickness of each layer is 2.5 nm—the expected thickness for the polymer in the preferred high-conductivity orientation. The smallest features we have written are about 75 nm wide, most likely limited by the sharpness of the current generation of cantilevers (which are relatively dull at approximately a 100-nm radius of curvature). Newer, sharper tips promise even finer features. Nonetheless, such exquisite control over polymer deposition—nanoscale widths and molecular layer thickness control—cannot be achieved by any other additive patterning method.

The large temperature range of the cantilevers, up to 1000 °C, allows many different inks to be used. Our exploration of high-melting-point inks has recently led to the writing of indium metal. As shown in Fig. 3, we have used tDPN to write narrow (< 80 nm) indium metal lines onto glass and silicon substrates. Though many methods have been used to create nanoscale metal lines, it is exceedingly difficult to make them continuously conductive. We wrote an In wire between gold electrodes and measured its resistance in NRL's unique Nanomanipulation and Nanocharacterization Facility. Ohmic contact was achieved, although the conductance was indicative of indium oxide (which is also a conductor). Nanoscale chemical analysis in the Facility confirmed the composition as indium oxide, as expected for an In nanowire deposited on a bench-top apparatus in laboratory air.

The Future for tDPN: Full realization of tDPN will require massively parallel lithography. Fortunately, arrays of 4,096 individually controlled thermal cantilevers, similar to ours, have already been fabricated by

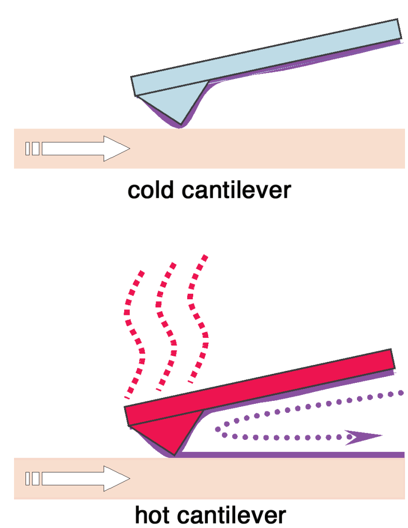

FIGURE 1
Scheme of Thermal Dip Pen Nanolithography. When the cantilever is cool, the ink is solid and does not flow. When the cantilever is heated, the ink melts and flows from the tip onto the surface. Moving the tip writes the ink pattern.

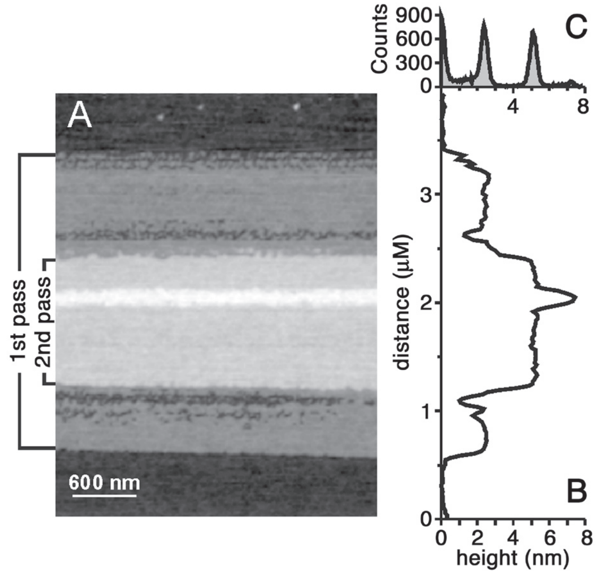

FIGURE 2
(a) Tapping-mode AFM image of a PDDT film deposited on SiO_2. The PDDT pre-coated tip was rastered at 5 µm/s with 47 nm/line while heated above PDDT's melting temperature. The outer pattern resulted from the first pass, which deposited a single monolayer. After 50 s, a second (rectangular) scan deposited a second monolayer without disturbing the first. (b) The average height profile; discrete height changes are apparent for each layer. (c) Height histogram of the film with peaks at 0, 2.4, 5.1, and 7.3 nm.

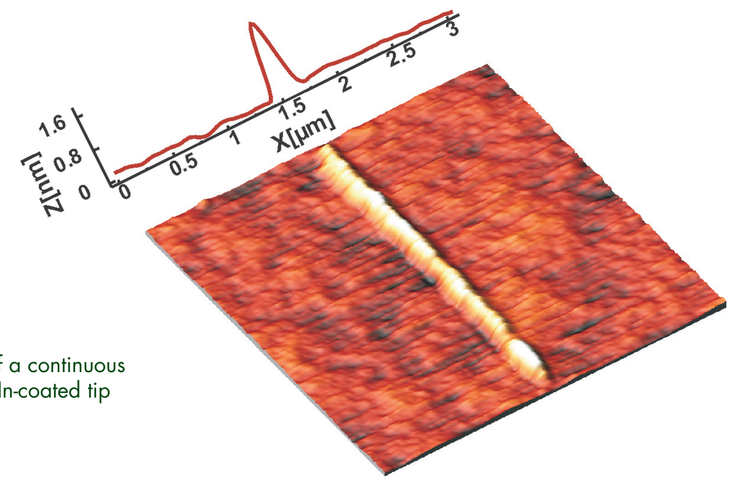

FIGURE 3
A topographic AFM image of a continuous nanowire deposited from an In-coated tip onto a glass substrate.

IBM for use in the "Millipede" memory storage system. Thermal cantilevers may be designed to give rapid heating (1 to 20 µs) and cooling (1 to 50 µs) times. Thus, rapid and highly parallel patterning of surfaces should be possible. Given tDPN's ability to deposit insulators, semiconductors, and conductors, it should one day be possible to write integrated circuits directly using an inexpensive, bench-top apparatus.

Although the immediate benefits of using a multipen tDPN to write integrated circuits will be nanoscale resolution and wafer-scale patterning, we expect many other benefits. For instance, unlike conventional fabrication methods, which etch away material to create small features, tDPN is an additive technique, which requires very little ink to create nanoscale devices. Therefore, the use of expensive inks can be kept to a minimum and the generation of toxic etchant wastes can be greatly reduced. Secondly, tDPN's robust deposition process enables the writing of many different materials onto many different substrates, a key capability needed for heterogeneous integration in microelectronics. Finally, multipen writing should be ideal for the fabrication of low numbers, hundreds to thousands, of integrated circuits without the billion-dollar development costs currently associated with integrated circuit fabrication. This capability, in particular, will be important to a low-volume, high-value customer such as the Department of Defense.

[Sponsored by DARPA and ONR]

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